IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Heer	Docket No.:	INF 2002 P 10624 US
Serial No.:	10/724,011	Art Unit:	2129
Filed:	November 26, 2003	Examiner:	Peter D. Coughlan
For:	Arrangement of Configurable Logic Blocks		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

This Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final Rejection mailed October 9, 2007. A Notice of Appeal was filed on February 11, 2008. A petition for a two-month extension of time is being submitted concurrently herewith.

REAL PARTY OF INTEREST (37 C.F.R. 41.37(c)(1)(i))

The present application is assigned to Infineon Technologies AG.

RELATED APPEALS AND INTERFERENCES (37 C.F.R. 41.37(c)(1)(ii))

Appellant filed an Appeal Brief on this same application on January 19, 2007. In response to that brief, prosecution was reopened.

STATUS OF CLAIMS (37 C.F.R. 41.37(c)(1)(iii))

Claims 1-14 stand finally rejected. No claims have been allowed. Therefore, claims 1-14 are the subject of this appeal. The claims on appeal are reproduced in the Claims Appendix.

STATUS OF AMENDMENTS (37 C.F.R. 41.37(c)(1)(iv))

No amendments have been filed since the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. 41.37(c)(1)(v))

The preferred embodiment of the invention provides a solution to the problem of minimizing the use of area for configurable logic blocks (CLB) and is achieved by adapting its corresponding components to the functional task of the CLB. Par. [0015], line 1, page 6. Thus, in the solution of the problem according to embodiments of the invention, a CLB contains a first and/or second look up table with content addressability, which implements the switching function of at least one conditional branch. Par. [0015], line 3, page 6. This conditional branch generates an "if then else" branch, which realizes a comparison of CLB input data with comparison data previously stored in the CLB. Par. [0015], line 6, page 6.

In a first aspect, as defined by claim 1, the invention provides a logic circuit that includes an input data node 1 for carrying input data. Par. [0024], line 1, page 8. A configurable logic block (CLB) control logic circuit 8 has a first input (coupled to input data node 1), a second input (coupled to control input node 10), a third input (coupled to comparator 6 or 16 of look-up table 2 or 12), a fourth input (coupled to multiplexer 3 or 13) and an output (coupled to node 11). At least one look up table 2 and/or 12, implements a

switching function of at least one conditional branch, with content addressability. Par. [0015], line 5, page 6.

The at least one look-up table 2 and/or 12 generates an "if then else" branch that realizes a comparison of the input data with comparison data previously stored in the at least one look-up table 2 and/or 12. Par. [0015], line 6, page 6. A result output of the at least one look up table 2 and/or 12 is provided to the third input of the CLB control logic 8. Par. [0026], line 3, page 9. For the look-up table 2, this third input can be seen as the second line from the bottom on the left-hand side of the CLB control logic circuit 8, which line came from the comparator 6 of look-up table 2.

An input data bus 7 is coupled between the input data node 1 and a bus input of the at least one look up table 2 and/or 12. Par. [0024], line 1, page 8. The bus input of the look-up table 2 is shown in the figure as the line going into look-up table 2 between register 4 and comparator 6. The first input of the CLB control logic circuit 8 is coupled to the input data node 1 via the input data bus 7. Par. [0024], line 5, page 8.

At least one multiplexer 3 and/or 13 has a control input coupled to the input data node 1 and also to the first input of the CLB control logic circuit 8 via at least part of the bit width of the input data bus 7. Par [0024], line 3, page 8. An output of the at least one multiplexer 3 and/or 13 is coupled to the fourth input of the CLB control logic circuit 8. Par. [0024], line 5, page 8. For the multiplexer 3, this third input can be seen as the third line from the bottom on the left-hand side of the CLB control logic circuit 8, which line came from the multiplexer 3.

A control input node 10 is coupled via a control bus 17 to the second input of the CLB control logic circuit 8. Par. [0024], line 6, page 9. This second input is shown as

connecting to the bottom of the block 8. At least one register data bus 5 is coupled between a register data bus output of the at least one look up table 2 and/or 12 and a bus input of the at least one multiplexer 3. Par. [0015], line 6, page 6.

In the embodiment of claim 2, the at least one look up table 2 and/or 12 is realized with the conditional branch implemented in it by such a switching function. Par. [0015], line 6, page 6. The at least one look up table 2 and/or 12 includes a register 4 which stores the comparison data and a comparator 6 coupled to the input data node and the register. Par. [0023], line 2, page 8. The comparator 6 is operable to compare the input data with the comparison data. Par. [0026], line 1, page 9.

In the embodiment of claim 3, the bus input of the at least one look up table 2 and/or 12 is coupled to a first bus input of the comparator 6 and/or 16 and wherein a bus output of the register 4 and/or 14 is coupled to a second bus input of the comparator 6 and/or 16 and also to the register data bus output of the at least one look up table 2 and/or 12. An output of the comparator 6 and/or 16 is coupled to the result output of the at least one look up table 2 and/or 12. Par [0026], line 1, page 9.

In the embodiment of claim 4 the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology. Par. [0028], line 2, page 10.

In the embodiment of claim 5, the output of the CLB control logic circuit 8 serves as an output of the CLB. Par [0026], line 6, page 9.

Claim 6 is the second independent claim. This claim recites a logic circuit that includes, a register 4, and a comparator 6 with a first input coupled to the register 4 and with a second input coupled to an input node 1. Par [0025], line 1, page 9. A multiplexer 8 with an input is coupled to the register 4. Par. [0025], line 3, page 9. A control block includes

inputs coupled to the multiplexer 3, the comparator 6, the input node 1 and a control input node 10. Par. [0026], line 4, page 9. The logic circuit realizes an "if then else" branch based upon information carried at the input node 1 and information stored in the register 4. Par. [0028], line 6, page 10.

In the embodiment of claim 7, the logic circuit comprises a configurable logic block. Par. [0028], line 2, page 10.

In the embodiment of claim 8, the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology. Par. [0028], line 2, page 10.

In the embodiment of claim 9, the logic circuit also includes, a second register 14, and a second comparator 16 with a first input coupled to the second register 14 and with a second input coupled to the input node 1. Par. [0025], line 3, page 9. A second multiplexer 13 includes an input coupled to the second register 14. Par. [0025], line 3, page 9. The control block 8 is coupled to the second comparator 6 and the second multiplexer 13. Par. [0026], line 4, page 9.

In the embodiment of claim 10, the output of the control block 8 serves as an output of the logic circuit. Par. [0026], line 6, page 9.

Claim 11 is the final independent claim. This claim recites a logic circuit that includes, means for performing a switching function of at least one conditional branch is implemented with content addressability. Par. [0015], line 5, page 6. The means for performing a switching function generates an "if then else" branch that realizes a comparison of input data with previously stored comparison data. *Id.* This embodiment also includes means for selecting at least a portion of the comparison data is coupled to the means for performing a switch function. Par. [0025], line 3, page 9. A CLB control logic circuit 8 has

a first input coupled to receive at least a portion of the input data, a second input coupled to the means for performing a switching function, and a third input coupled to the means for selecting. Par. [0026], line 1, page 9.

Claim 11 includes means-plus-function language in accordance with 35 U.S.C. § 112, sixth paragraph. The means for performing a switching function can be implemented by lookup table 2. Par. [0015], line 5, page 6. The means for selecting can be implemented by multiplexer 3. Par. [0025], line 3, page 9.

In the embodiment of claim 12, the means for performing a switching function comprise, means for storing the comparison data (e.g., register 4) and means for comparing the comparison data and the input data (e.g., comparator 6). Par. [0025], line 1, page 9.

In the embodiment of claim 13, the means for performing a switching function comprises a register 4 that stores the comparison data and a comparator 6 coupled to the register and to an input data node 1 that carries the input data. Par. [0025], line 1, page 9.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. 41.37(c)(1)(vi))

(1) Claims 1-14 stand objected to based on the drawings.

(2) Claims 1-14 stand rejected under 35 U.S.C. § 101 for non- statutory subject matter.

(3) Claims 1-14 stand rejected under 35 U.S.C. § 112, first paragraph, because current case law require such a rejection if a 101 rejection is given.

ARGUMENT (37 C.F.R. 41.37(c)(1)(vii))

It is respectfully submitted that claims 1-14 recite patentable subject matter under the provisions of 35 U.S.C. §§ 101 and 112. Further, the drawings clearly show the claimed invention.

Each of the three rejections listed above are based on the same rationales. Accordingly, all three will be discussed together.

While the Examiner has presented numerous specific objections, Appellant believes the crux of the rejection is provided on page 6 of the Final Rejection, which states "[t]he invention as described within the specification and only diagram will not work as equivalent to an 'if-then-else' statement." Each of the specific rejections really boil down to this one point, whether the claimed invention as described in the present application will work.

As described in the Summary section above, the claimed invention is clearly described in the application. This question is not debated. Further, however, Appellant respectfully submits that one of ordinary skill in the art would be able to implement the claimed circuitry based on the teachings of the present application. As a result, Allowance is respectfully requested.

Each of the specific points raised in the Final Rejection will now be addressed.

Logic Circuit

Claims 1, 5, 6, 7, 10, 11, 14 have been objected to "based on all these claims pertain to the 'logic circuit' (item 8)." The rejection states:

> Concerning Control Block (item 8). According to the diagram there are 6 inputs (none of which is a clock input, see below) and a single output. There is no diagram which illustrates the internal circuit which discloses the logic how the output (item 11) is reached. The diagram and specification are silent regarding the contents of item 8. This non-description reasoning of that

output 11 is correct is not acceptable. There needs to be some diagram which discloses the internal workings of item 8. [page 3; *see also* page 7]

Appellant agrees that CLB control logic 8 shows six inputs and one output. The real question being raised is whether the present application provides an enabling description of the present invention. Appellant respectfully submits that one of ordinary skill in the art reading the present application would be enabled to make and use the invention defined by the claims of the present application.

Appellant respectfully submits that one of ordinary skill in the art would know how to implement the CLB control logic 8 based upon the teachings of the present invention. The sequential functions of the configurable logic blocks (CLB) are executed by sequential CLB control logic, whose memory elements represent D-FFs. Par. [0007]. As explained in the application, the combinatorial circuit part of a common configurable logic block (CLB) consists of look up tables (LUT), which are preferably realized by static RAM. Par. [0006]. Arbitrary combinatorial functions, which are represented by truth tables, are converted into these look up tables. *Id.* For these truth tables, one also speaks of function tables, which can be realized by matrix memories and expanded, e.g., by multiplexers, or just by the memories alone. *Id.*

An advantage, according to embodiments of the invention, is provided for the implementation of more than one conditional branch in an LUT, where an additional savings of hardware resources is achieved by reducing the required CLBs. Par. [0021]. Since it is guaranteed that the comparison data, which are stored in the LUT and which are required for processing with the CLB controller, are also simultaneously already available for further processing in typical multiplexers of a CLB. *Id.* Therefore, additional hardware, which would otherwise be necessary, is likewise spared for each CLB that is used. *Id.*

The teachings of the specification and drawings provide sufficient information for one of ordinary skill in the art to implement the invention. As to the drawing itself, Appellant respectfully submits that a box is sufficient to illustrate the claimed control logic block.

The Final Rejection also states the following:

> Concerning input 10 in which the applicant states that 'The specification never states that control input 10 is limited to a clock signal nor that the second input of the CLB control logic 8 is limited to a clock input.' The applicant is correct with this statement and the Examiner made this conclusion based on the fact that the triangle shape in item 8 is standard notation which represents a clock input. This is widely used for example, looking at the EP 0410759A2 (which is supplied by the applicant) which shows FF1 and FF2 with the triangle shape being connected to K Clock. Applicant now states on the record that there is no clock input on the invention. [page 7]

In the Amendment dated August 7, 2007, Appellant stated that "[t]he specification never states that control input 10 is limited to a clock signal nor that the second input of CLB control logic 8 is limited to a clock input." Appellant stands by this statement but has never stated that there is no clock input on the invention. Further, Appellant cannot see why this discussion is remotely relevant since no clock is ever claimed. The so called clocked output of the control circuit 8 is standard design practice and not claimed as part of the invention.

Multiplexer

Claims 1, 6 and 9 have been objected to due to the input parameters of the multiplexer. Appellant will address each of the issues raised in the Final Rejection.

> For example item 1 is input which consists of 1-n input values. These inputs go to comparator 6 (and 16) and also to multiplexer 3 (and 13). It is known within the art that multiplexers have 2 different inputs, but these are not labeled within the diagram. [Final Rejection, pages 3-4; *see also* pages 6-7]

Appellant respectfully submits that the multiplexer is clearly labeled such that one of ordinary skill in the art would understand the operation thereof. The bus inputs of the multiplexer 6 are very clearly shown as being received from the register 4. Par. [0025], which states that comparison data, which are stored in the register 4, are led to the register data bus output of the look-up table 2 and are switched over a corresponding first or second register data bus 5 to the bus input of the first multiplexer 3. The control inputs of the multiplexer are very clearly shown as being received from the input 1. Par. [0024], which states that data from data input 1 are led in one part of the bit width of the input data bus 7 to the corresponding multiplexer control input of the multiplexer 3.

This operation is in fact a fundamental function of a CLB within FPGAs as known by those of ordinary skill in the art. As quoted above, the "... data from input 1 are led in one part of the bit width of the input data bus 7 to the corresponding multiplexer control input for multiplexer 3...". This multiplexer is for example selected by, e.g., 3 bit of a, e.g., 8 bit input bit width on bus 7. These 3 bit control multiplexer 3 and select one out of the 8 stored bits from reference word in register 2. The same happens within multiplexer 13, but controlled by ***different*** e.g. 3 bit from bus 7. The rest of bus 7 (usually 1 or 2 bit) is directly connected to the output control block 8. In this example, each multiplexer would have 8 inputs and a 3-bit selection signal. Each of these facts would be well known to one that understands FPGAs.

> In addition the number of inputs for these two types of inputs do not have the same number of inputs. But according to the diagram there are the same number of inputs going to the comparator as to the multiplexer and there are the same number of inputs coming from the comparator as to the multiplexer. Thus the multiplexer is getting the same number of inputs from the input (item 1) and from the comparator (item 6) which can't happen at all. The statement within the specification, 'Simultaneously, these data are led in one part of the bit width of the input data bus 7 to the corresponding multiplexer

> control input of the first and/or second multiplexer 3' does not make sense and looking at the diagram, it makes no sense to do this function. [Final Rejection, page 4; *see also* page 7]

Appellant is confused as to the question since it appears to be factually inaccurate. The diagram never shows the same number of inputs going to the comparator as to the multiplexer. The comparator 6 clearly receives inputs from the data input 1 and from the register 4. The multiplexer 3 receives bus inputs from the register 4 and also receives control inputs from the data input 1, as quoted in the final rejection, from a part of the bit width of data bus 7.

Appellant respectfully submits that the drawing is self-explanatory even without the corresponding text. The Final Rejection's statement that the diagram makes no sense is unfounded. Appellant respectfully submits that the diagram would make perfect sense to one of ordinary skill in the art.

In response to earlier prosecution, the Final Rejection states:

> [T]here are three regions within a multiplexer. One of these regions is call the 'selector' (or 'controller'). Since the applicant refuses to follow standard circuit diagrams, and the explanation of ¶0024 does not go into detail concerning the selector (or controller), the Examiner cannot determine the function of the drawing from the drawing itself or the specification. [page 11]

Paragraph 24 very clearly states that data from data input 1 are led to the corresponding ***multiplexer control input*** of the multiplexer 3.[1] Certainly, the Examiner can determine the function of the drawing. Appellant respectfully submits that the control input of the multiplexer is very clear.

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[1] The next paragraph provides the full quotation.

In the next section of page 11 of the Final Rejection, the Examiner states that the statement in Paragraph 24 "makes no sense." The statement in question reads, "Simultaneously, these data are led in one part of the bit width of the input data bus 7 to the corresponding multiplexer control input of the first and/or second multiplexer 3; 13 and also to the first input of the CLB control logic 8." Referring to the Figure, it is clear that input 1 is connected to both the control input of the multiplexer 3 and an input of CLB control logic 8. As a result, any data present on this line would simultaneously be led to both of these places. Appellant respectfully submits that this circuit makes perfect sense.

Comparator Circuit

Claims 2, 3, 6, 9, 12 and 13 have been objected to based on the lack of description of the comparator circuit. Appellant respectfully submits that the comparator circuit is clearly described. The LUTs each have a first or second comparator 6 or 16 comparing the input data with the stored comparison data, i.e., from register 4 or 14. Par. [0019]. Appellant respectfully submits that this description is sufficient to one of ordinary skill in the art to understand the function of a comparator.

The rejection goes on to ask a number of questions,[2] in particular:

- What type of 'comparator' is being used?

Any comparator known in the art can be used. The specification is not limited.

- Are they 'and' gates, 'or' gates, 'nor' gates or some combination of standard thereof?

Any of these logical constructs can be used to implement the comparator. The specification is not limited.

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[2] *See* page 4 of the Final Rejection for the questions. *See also* page 8.

- Worded another way, 'and', 'nand', 'or' or 'nor' gates each have their own corresponding truth table. What is the truth table for the 'comparator' circuit?

Any specific implementation of a truth table can be used. The specification is not limited. The truth table is trivial.

Appellant notes that the specific questions raised in the Final Rejection provide further evidence that one of ordinary skill in the art would know how to implement a comparator. Appellant respectfully submits that comparators are well known in the art and one of ordinary skill would understand how to implement a comparator in the context of the present invention.

Means for Storing the Comparison Data

Claim 12 has been objected to based on the assumption of the ability to 'storing the comparison data.' The Figure clearly shows a register 4, which is an example of a means for storing comparison data. Appellant respectfully submits that a register has the ability to store data.

> An additional problem with the diagram is how do the registers get initialized with initial values so that they can be used in conjunction with the comparators? Per the specification Par. 0006 these registers or 'look up tables' are composed of RAM. RAM needs to be initialized. There is no input to these registers or 'look up tables.' [page 5, *see also* page 8]

The Final Rejection notes that no input is shown for the registers as this is well known in state of the art FPGA design. Appellant respectfully submits that no input is claimed and, as a result, no input need be shown. One of ordinary skill in the art would clearly understand how to initialize a memory by storing comparison data therein. Typically, the register is initialized at boot-up of the system and the inputs are inactive

during operation and, therefore, not relevant for the application. Specific teaching of such a clearly well known unclaimed task is not required.

Input Output Parameters and Connections

Claims 4 and 8 are objected to based on lack of input and output parameters and associated connections of registers, comparators, multiplexers, and control logic circuits. Appellant respectfully submits that each of the claimed inputs, outputs and connections are clearly shown in the drawing and described in the specification. One of ordinary skill in the art would unquestionably be able to construct the claimed logic circuit.

The Final Rejection goes on to state:

> A FPGA acts like a ASIC only with different performance properties and turn around time. A circuit is a circuit regardless of other characteristics. There exists a problem with the overall design of the invention as well. Per the specification the circuit realizes an 'if then else' branch.
>
> A 'if then else' design has three main components, 'Statement A', 'result B' and 'result C.' It works by if 'Statement A' is true then 'result B' is outputted and if 'Statement A' is false then 'result C' is outputted. Therefore there are 3 registers needs to realize an 'if then else' branch. One for 'Statement A', 'result B' and 'result C'. The invention only has two registers. Also there is only one comparison ('Statement A'), but the invention has two comparators, which makes no sense. There needs to be only one multiplexer but the invention has two of them. The output of the comparator needs to control the multiplexer, but in the invention the output of the comparators lead to a control logic in which nothing is described within the specification.
>
> The Examiner cannot assume connections and possible functions for given items within the diagram and lack of explanation within the specification. With this in mind, the Examiner cannot see how the invention works. [pages 5-6; *see also* pages 8-9]

The Final Rejection states that the invention requires three registers. Appellant respectfully disagrees. There is nothing in the claims that limits 'result B' and 'result C' from being stored in the same register. There is nothing in the claims that limits 'result B' and

'result C' from being received at the input 1. There is nothing in the claims that forbids a combination of these. The same holds true for the operands of any comparison.

As an example, one of ordinary skill in the art would recognize that the invention can implement the if-then-else in the following manner. Input data word 1 is applied via bus 7 in full bit width to the comparator 6 and/or 16. The second input of the comparator is in full bit width connected to the reference data register 4 and/or 14. The comparators 6/16 fulfill a bit-wise boolean and-function. Therefore if all individual bits of input data word 1 equal the stored reference in register 2/12, the output of the comparator 6/16 is a boolean "1", if one or more bits of input data word 1 do not equal the respective bit of the stored reference in register 2, the output of the comparator is a boolean "0". This procedure, therefore, clearly implements an "if-(word 7 equal word 2)-then-("1")-else-("0")" function.

The Final Rejection also states that only one comparator is necessary but two are shown. Assume, for the sake of argument, that it is correct that only one comparator is necessary. Either of the two illustrated comparators 6 or 16 could then perform the needed function. The same logic holds true for the multiplexer.

Once again the question is whether one of ordinary skill in the art would be enabled to make and use the invention defined by the claims of the present application. The teachings are unambiguous. The claims are clear. As a result, one would be enabled to make and use the present invention. Each of the questions raised in the Final Rejection are clearly answered in the specification of the present invention.

CONCLUSION

For the foregoing reasons, Appellant respectfully submits that the final rejection of the pending under 35 U.S.C. § 101 and 112 is improper and respectfully requests that the Board of Patent Appeals and Interference so find and reverse these rejections.

To the extent necessary, Appellant petitions for an Extension of Time under 37 C.F.R. § 1.136. Please charge any fees, or credit any overpayments, in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 50-1065.

Respectfully submitted,

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CLAIMS APPENDIX

1. A logic circuit comprising:

an input data node for carrying input data;

a configurable logic block (CLB) control logic circuit having a first input, a second input, a third input, a fourth input and an output;

at least one look-up table in which a switching function of at least one conditional branch is implemented with content addressability, wherein the at least one look-up table generates an "if then else" branch that realizes a comparison of the input data with comparison data previously stored in the at least one look-up table, and wherein a result output of the at least one look-up table is provided to the third input of the CLB control logic circuit;

an input data bus coupled between the input data node and a bus input of the at least one look-up table, wherein the first input of the CLB control logic circuit is coupled to the input data node via the input data bus;

at least one multiplexer having a control input coupled to the input data node and also to the first input of the CLB control logic circuit via at least part of the bit width of the input data bus, an output of the at least one multiplexer being coupled to the fourth input of the CLB control logic circuit;

a control input node coupled via a control bus to the second input of the CLB control logic circuit; and

at least one register data bus coupled between a register data bus output of the at least one look-up table and a bus input of the at least one multiplexer.

2. The circuit of claim 1, wherein the at least one look-up table is realized with the conditional branch implemented in it by such a switching function, and wherein the at least one look-up table comprises:

a register which stores the comparison data; and

a comparator coupled to the input data node and the register, the comparator operable to compare the input data with the comparison data.

3. The circuit of claim 2 wherein the bus input of the at least one look-up table is coupled to a first bus input of the comparator and wherein a bus output of the register is coupled to a second bus input of the comparator and also to the register data bus output of the at least one look-up table, and wherein an output of the comparator is coupled to the result output of the at least one look-up table.

4. The circuit of claim 1 wherein the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology.

5. The circuit of claim 1 wherein the output of the CLB control logic circuit serves as an output of the CLB.

6. A logic circuit comprising:

a register;

a comparator with a first input coupled to the register and with a second input coupled to an input node;

a multiplexer with an input coupled to the register; and

a control block with inputs coupled to the multiplexer, the comparator, the input

node and a control input node, wherein the logic circuit realizes an "if then else" branch based upon information carried at the input node and information stored in the register.

7. The circuit of claim 6 wherein the logic circuit comprises a configurable logic block.

8. The circuit of claim 7 wherein the configurable logic block is realized in Field Programmable Gate Array (FPGA) technology.

9. The circuit of claim 6 and further comprising:

a second register;

a second comparator with a first input coupled to the second register and with a second input coupled to the input node;

a second multiplexer with an input coupled to the second register; and

wherein the control block is coupled to the second comparator and the second multiplexer.

10. The circuit of claim 6 wherein the output of the control block serves as an output of the logic circuit.

11. A logic circuit comprising:

means for performing a switching function of at least one conditional branch implemented with content addressability, wherein the means for performing a switching function generates an "if then else" branch that realizes a comparison of input data with previously stored comparison data;

means, coupled to the means for performing a switch function, for selecting at least a portion of the comparison data; and

a CLB control logic circuit having a first input coupled to receive at least a portion of the input data, a second input coupled to the means for performing a switching function, and a third input coupled to the means for selecting.

12. The circuit of claim 11 wherein the means for performing a switching function comprises:

means for storing the comparison data; and

means for comparing the comparison data and the input data.

13. The circuit of claim 11 wherein the means for performing a switching function comprises:

a register that stores the comparison data; and

a comparator coupled to the register and to an input data node that carries the input data.

14. The circuit of claim 11 wherein the logic circuit is realized in Field Programmable Gate Array (FPGA) technology.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None